AMENDMENTS TO THE CLAIMS

Listing of the claims:

Following is a listing of all claims in the present application, which listing supersedes all previously presented claims:

1. (Previously Presented) A MOS-type solid-state image pickup device comprising:

a semiconductor substrate;

a large number of pixels arranged in one surface of said semiconductor substrate in an array having a plurality of rows and a plurality of columns, each said pixel including (a) a photoelectric converter element having a cathode and (b) a switching circuit electrically connected to said cathode of the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode;

a plurality of row selection signal lines disposed along a row direction, each being associated with one pixel row for supplying a row selection signal;

a plurality of output signal lines disposed along a column direction, each being associated with at least one pixel column;

a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal;

a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having no random access function;

TECH/531525.1

a power source line; and

an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time;

wherein said switching circuit comprises:

a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and

a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line.

2-3. (Canceled).

4. (Currently Amended) A MOS-type solid-state image pickup device according to claim 1, further comprising:

~~a readout row shifter for sequentially supplying the row selection signal to said row selection signal lines;~~

~~a reset row shifter for sequentially supplying the reset signal to said reset signal lines; and~~

an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal.

5. (Previously Presented) A MOS-type solid-state image pickup device according to claim 4, wherein said image signal outputting device comprises:

at least one analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal; and

a row-directional shifter for controlling operation of said analog signal generator and for sequentially outputting the analog voltage signal from said at least one analog signal generator.

6. (Previously Presented) A MOS-type solid-state image pickup device according to claim 4, wherein said image signal outputting device comprises:

an analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal;

an analog-to-digital converter for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and

a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom.

7. (Currently Amended) A MOS-type solid-state image pickup device according to claim 4, further comprising a controller for controlling operations of said overall reset controller, said row read scan circuit ~~readout row-shifter~~, said reset scan circuit ~~row-shifter~~, and said image signal outputting device.

8. (Previously Presented) A MOS-type solid-state image pickup device according to claim 1, further comprising:

a transfer signal line disposed for each said pixel row; and

a transfer control row-shifter for sequentially supplying a transfer control signal to said transfer signal lines, and

each said switching circuit further comprises a transfer transistor electrically connected between said cathode and the gate of said output transistor, which gate is also connected to said reset transistor, said transfer transistor including a control terminal electrically connected to said transfer signal line.

9. (Canceled)

10. (Currently Amended) A MOS-type solid-state image pickup device according to claim 8, further comprising:

~~a readout row-shifter for sequentially supplying the row-selection signal to said row-selection signal lines;~~

~~a reset row-shifter for sequentially supplying the reset signal to said reset signal lines; and~~

an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal.

11. (Previously Presented) A MOS-type solid-state image pickup device according to claim 10, wherein said image signal outputting device comprises:

at least one analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal; and

a row-directional shifter for controlling operation of said analog signal generator and for sequentially outputting the analog voltage signal from said analog signal generator.

12. (Previously Presented) A MOS-type solid-state image pickup device according to claim 10, wherein said image signal outputting device comprises:

an analog signal generator for converting the output signal generated on each said output signal line into an analog voltage signal;

an analog-to-digital converter for receiving the analog voltage signal and for converting the analog voltage signal into a digital signal; and

a buffer memory for receiving the digital signal, temporarily keeping the digital signal therein, and outputting the digital signal therefrom.

13. (Currently Amended) A MOS-type solid-state image pickup device according to claim 10, further comprising a controller for controlling operations of said overall reset controller, said row read scan circuit ~~readout row-shifter~~, said reset scan circuit ~~row-shifter~~, said transfer control row-shifter, and said image signal outputting device.

TECH/531525.1

14. (Previously Presented) A digital camera, comprising:

a MOS-type solid-state image pickup device comprising:

(i) a semiconductor substrate;

(ii) a large number of pixels arranged in one surface of said semiconductor substrate in an array having a plurality of rows and a plurality of columns, each said pixel including (a) a photoelectric converter element having a cathode and (b) a switching circuit electrically connected to said cathode of the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode;

(iii) a plurality of row selection signal lines disposed along a row direction, each being associated with one pixel row for supplying a row selection signal;

(iv) a plurality of output signal lines disposed along a column direction, each being associated with at least one pixel column;

(v) a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal;

(vi) a readout row-shifter for sequentially supplying the row selection signal to said row selection signal lines;

(vii) a reset row-shifter for sequentially supplying the reset signal to said reset signal lines;

(viii) an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time;

(ix) a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan

TECH/531525.1

circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having no random access function;

(x) an image signal outputting device electrically connected to said output signal lines for generating an image signal representing the output signal and for sequentially outputting the image signal; and

(xi) a power source line;

wherein said switching circuit comprises:

a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and

a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line;

an image signal processor for generating mobile picture data or still picture data using the image signal outputted from said MOS-type solid-state image pickup device;

a light shielding device for interrupting light incident to said MOS-type solid-state image pickup device;

a still picture indication signal generator for generating a still picture indication signal indicating shooting of a still picture;

a mobile picture mode controller electrically connected to said MOS-type solid-state image pickup device for continually control operation thereof for repeatedly conducting (a) an image readout operation in which the row selection signal is

TECH/531525.1

sequentially supplied from said readout row-shifter to a predetermined number of row selection signal lines for sequentially outputting from said image signal outputting device an image signal representing the output signal generated on each said output signal line and (b) an electronic shutter operation in which the reset signal is sequentially supplied from said reset row-shifter to said reset signal supply lines at least associated with said pixel row as an object of the image signal readout operation for sequentially discharge electric charge accumulated in said photoelectric converter elements; and

a first still picture mode controller electrically connected to said MOS-type solid-state image pickup device for controlling in place of said mobile mode controller, when the still picture indication signal is outputted, operations of said MOS-type solid-state image pickup device and said light shielding device, for conducting an overall reset operation in which the overall reset controller is operated, in a state in which the operations of said readout row-shifter and said reset ~~rest~~ row-shifter are stopped, and electric charge accumulated in all said photoelectric converter elements is discharged, and for conducting an image signal readout operation in which said light shielding device is operated and interrupts the incident light for a predetermined period of time after the overall reset operation is finished, and the row selection signal is sequentially supplied from said readout row-shifter to said row selection signal lines for sequentially outputting an image signal representing the output signal generated on said output signal lines from said image signal outputting device.

15. (Previously Presented) A digital camera according to claim 14, wherein:

when an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, said first still picture mode controller does not interrupt the operation; and

when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, said first still picture mode controller conducts the image signal readout operation once after the electronic shutter operation; and then the first still picture mode controller conducts the overall reset operation.

16. (Previously Presented) A digital camera according to claim 14, wherein said MOS-type solid-state image pickup device further comprises:

a transfer signal line disposed for each said pixel row; and

a transfer control row-shifter for sequentially supplying a transfer control signal to said transfer signal lines, and

each said switching circuit further comprises

a transfer transistor electrically connected between said cathode and the gate of said output transistor, which gate is also connected to said reset transistor,

said transfer transistor including a control terminal electrically connected to said transfer signal line

said mobile picture mode controller or said first still picture mode controller conducting said transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each said transfer signal lines associated with said pixel row as an object of the operation.

TECH/531525.1

17. (Previously Presented) A digital camera according to claim 14, further comprising:

a strobe device for emitting flash light when a predetermined signal is received or said strobe device installing device for installing therein;

a second still picture mode controller electrically connected to said MOS-type solid-state image pickup device for controlling in place of said mobile mode controller, when the still picture indication signal is outputted, operations of said MOS-type solid-state image pickup device and said light shielding device, for conducting an overall reset operation in which the overall reset controller is operated, in a state in which the operations of said readout row-shifter and said reset row-shifter are stopped, and electric charge accumulated in all said photoelectric converter elements is discharged, and for conducting an image signal readout operation in which after the overall reset operation is finished, a strobe device operation signal is generated for operating said strobe device; said light shielding device is operated and interrupts the incident light for a predetermined period of time after said strobe device operation signal is generated; and the row selection signal is sequentially supplied from said readout row-shifter to said row selection signal lines for sequentially outputting an image signal representing the output signal generated on said output signal lines from said image signal outputting device; and

a still picture mode specifying device for specifying, beforehand, a still picture mode controller to be operated when the still picture indication signal is outputted.

18. (Previously Presented) A digital camera according to claim 17, wherein:

TECH/531525.1

when an electronic shutter operation or an image signal readout operation is being executed at a point of time when the still picture indication signal is outputted, said second still picture mode controller does not interrupt the operation; and

when an electronic shutter operation is being executed at a point of time when the still picture indication signal is outputted, said second still picture mode controller conducts the image signal readout operation once after the electronic shutter operation; and then the second still picture mode controller conducts the overall reset operation.

19. (Previously Presented) A digital camera according to claim 17, wherein said MOS-type solid-state image pickup device further comprises:

a transfer signal line disposed for each said pixel row; and

a transfer control row-shifter for sequentially supplying a transfer control signal to said transfer signal lines, and

each said switching circuit further comprises

a transfer transistor electrically connected between said cathode and the gate of said output transistor, which gate is also connected to said reset transistor,

said transfer transistor including a control terminal electrically connected to said transfer signal line.

said mobile picture mode controller, said first still picture mode controller or said second still picture mode controller conducting said transfer control row-shifter for sequentially supplying, in the image readout operation, the row reset operation, or the overall reset operation, the transfer control signal to each said transfer signal lines associated with said pixel row as an object of the operation.

TECH/531525.1

20. (Previously Presented) A MOS-type solid-state image pickup device comprising:

a semiconductor substrate;

a large number of pixels arranged in one surface of said semiconductor substrate in an array having a plurality of rows and a plurality of columns, each said pixel including (a) a photoelectric converter element having a cathode and (b) a switching circuit electrically connected to said cathode of the photoelectric converter element for controlling generation of an output signal representing electric charge accumulated in said cathode and discharge of the electric charge from said cathode;

a plurality of row selection signal lines disposed along a row direction, each being associated with one pixel row for supplying a row selection signal to select pixels of the associated pixel row;

a plurality of output signal lines disposed along a column direction, each being associated with at least one pixel column for supplying output signals of the pixels selected by the row selection signal;

a plurality of reset signal lines disposed along the row direction, each being associated with one pixel row for supplying a reset signal to clear the pixels of the associated pixel row;

a row shift circuit including a row read scan circuit capable of supplying a read signal to said plurality of row selection signal lines sequentially, and a reset scan circuit capable of supplying a reset signal to said plurality of reset signal lines sequentially, the row shift circuit having no random access function;

a power source line; and

an overall reset controller for supplying an overall reset signal to all of said reset signal lines at one time;

wherein said switching circuit comprises:

a series connection of an output transistor and a selection transistor connected between the power source line and an associated output signal line, the output transistor having a gate being capable of receiving a potential generated by the charge accumulated in said cathode, the selection transistor having a gate connected to an associated row selection signal line; and

a reset transistor connected between said cathode and said power source line, and having a gate connected to an associated reset signal line.

TECH/531525.1